VLSI / Embedded System Trainer (XPO - EST)
(CPLD / FPGA / 89C51 / PIC / ARM etc.)

Salient Features

- Aesthetically designed Injection moulded Plastic enclosure.
- XPO series of Embedded trainers VIZ; CPLD, FPGA, 89C51Rd2, PIC, 68HC11 etc.
- Supports use of 5V tolerant ICs (FPGA etc.) obviating need of special precautions by students.
- Set of Users Guide provided with each unit with emphasis on C Programming as well as assembly language programming.
- In circuit system programming **(ICSP)** supported through PC ports of COM/LPT.
- Can interface to application boards of XPO series microprocessor trainers saving customer investment.

Technical Specifications :

Following Onboard Resources are offered for experimentation however not every resource can be used fully with particular ECU due to paucity of its IO capacity.

User Manual	Set of Manuals: Student Workbook, Instructor Guide and technical Reference, Sample programs on Floppy/CD.
Speed	16 MHz crystal operated multi-output clock source to operate various resources on Mother Board like CPU, Baud rate, T/C etc.
I/O Pins	48 I/O lines through 2 Nos. of 26 pin FRC header.
Serial Interface	RS-232c serial interface using RS232 driver IC through 9 Pin male D connector.
Parallel Interface	25 pin male D connector for Parallel interface for JTAG based programming.
Display (Option)	16 × 2 LCD (Backlit) | 20 x 4 LCD (Backlit)
Key Board	Keyboard interface to support 101 Keys PC AT Keyboard. [PC Keyboard Not included in the scope of supply.]
Battery Backup	Rechargeable NiCd battery (3.6/60maH) provided to supply power to battery backup memory where ever needed.
Additional Resources	♣ Ext. L/S (8Ω/0.5W) I/F for experiments on frequency synthesis. ♣ Reset push button. ♣ Programmable Wait state generator . ♣Variable Slow CLK(2Hz-64Hz) provided for internal timers/counter functions applications. ♣ Pot varying between 0 -5V to simulated variable analog I/P to the built in ADC channels wherever applicable. ♣ General purpose bicolor (green,red) 8 x 2 LEDs & 8 Push Button Switches. ♣ Bread board with 400 tie points (83 mm x 54 mm) (optional) ♣ I2C based 24C512 (EEPROM), DS1307(RTC) and SPI based 93C46 (EEPROM) (optional)
ISP cables	1) 9 pin Female to 25 pin male RS-232C cable 2) 26 pin FRC IO cable 3) 25 pin female to 25 pin male for Parallel Interface
Power Supply	5V regulated through Jack provided on MB. 1.8V/2.5 V and 3.3V are additionally generated onboard for CPLD/FPGAs.
Mechanical Details	Aesthetically designed Injection moulded plastic enclosure of size 215(L) × 165(W) × 75(H) mm. Weight = 900 gm.(1.5 Kg with manuals)

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P.T.O.

Choice of Embedded Controller ECU Specifications :-

CONTROLLER DEVICE	MC68HC11E9/E1*	89C51RD2	16F877 (Pic)	CPLD XC95108	FPGA XC2S50	CPLD * MAX 7128	FPGA * ACEX 1K50	IspGAL *	ARM LPC2103/4/5/6	ARM LPC2138
Manufacturer	Motorola	Atmel / Philips	Mircochip	XILINX	XILINX	ALTERA	ALTERA	LATTICE	PHILIPS	PHILIPS
PACKAGE	52 pin PLCC	40 pin DIP package	40 Pin DIP	PLCC 84 pin	PQ 208 pin	PLCC 84 pin	TQ 144 pin	28 pin PLCC	LQFP48(SMD)	LQFP64(SMD)
CAPACITY ON CHIP RAM FLASH/EEPROM	 512 Bytes 512 Bytes	 256 Bytes data RAM 8 KBytes	 256 Bytes 8KB	 108 Macrocells 1600 gates	 CLBs 50K gates	 128 Macrocells 5000 gates	 CLBs 50K gates	 10 OLMCs	 8 KBytes 32 KBytes	 32 KBytes 512KBytes
OPERATING FREQ.	8 MHz	16 MHz	4 MHz	16 MHz	16 MHz	16 MHz	16 MHz	-	14 MHz	14 MHz
I/O CAPACITY	5 X 8 I/O ports (40)	4 X 8 I/O ports. (32)	24 + 9 I/O	36+26	36+26	36+26	36+26	12 I/P+10 IO	32	47
OPERATING SYSTEM ICSP S/W PC PORT	Window / XP WinBug11 Com Port	Window / XP WinIsp Com Port	Window / XP PIC Boot loader Com Port	Window / XP Xilinx web pack parallel port JTAG		Window / XP Altera Quartus III web pack parallel port JTAG		Galblast.exe Parallel port	winXP Isp soft.-Philips Com port or JTAG	winXP Isp soft.-Philips Com port or JTAG
SPECIAL PURPOSE IOs	2 Nos. XIRQ /, IRQ	7 interrupt sources, depending on device.	3* 16 bit TC 14 Ints	Global clock with low skew and global set / reset				-	10 Bit ADC 4 PWM	10 Bit ADC, DAC 1 PWM
EXECUTION METHOD	From internal RAM	From Flash	From flash	From Flash	From SRAM	From Flash	From SRAM	From JEDEC fuse map	From Flash	From Flash
PROGRAMMING LANGUAGE +	C Language or Assembly Language	C Language Assembly Language	C Language (Optional) Assembly Language	VHDL/ VERILOG However listing provided in users guide follows VHDL.				-	IDE - Any edit, GNURAM C Language & assembly tools	

+ We supply free on CD webpacks / evaluation software. The responsibility of using licensed software version lies with users wherever applicable. *** Consult factory**

Application Boards (Optional) : **Note :** All ECUs may not be capable of driving following Application boards in totality on account of their memory, IO, resource limitation.

1) Traffic light of 2 intersections cum logic study card with 24 tags and 24 LED's.

2) Stepper motor and 12V DC Motor Interface card with motors mounted in it to illustrate speed, direction control.

3) Scanning Techniques illustrating 8×8 LED Matrix,4×4 Keypad, 7 segment 8 digit red LED display study card.

4) Temperature Controller with MINI OVEN with 8 bit ADC- 8 bit DAC cum Instrumentation Opamp study card.

5) Opto-isolated 24 Vdc 12 Input and 10 Output IO card with additional 2 relay output study card.

6) 8bit 8 channel SAR ADC (unipolar) DAC (0-5V/±5V). Optional - Digital gain amplifier with built-in L/S interface Electret microphone with preamplifier, light sensor, Analog bar graph (0-5V), voice sampling and replay (optional).